

ABSTRACT

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A method and processor for FIR filtering a series of real input values with a series of filter coefficients where each of the input values is loaded from memory into the processor, and the processor employs each loaded input value in computing more than one
10 filter output value at a time, whereby the amount of data which needs to be transferred between memory and the processor is substantially reduced. The filter output values are preferably real data values, although the invention could be adapted to operate on complex number pairs. More than one input value can be loaded from memory in each clock cycle. Computations can be made by a multiply-and-accumulate unit, within a filtering
15 unit with dedicated hardware within the processor, or by a general-purpose digital signal processor (DSP). By using existing units within the processor, little or no modification is required to the processor in order to achieve a substantially improved performance.